ELECTRON TUBES

RCA Application Note

AN-160

Use of Point-Contact Transistors In Switching Service

This Note describes the input and output characteristics of point-contact transistors and shows how to utilize these characteristics to best advantage in basic switching applications.

Input Characteristic

The "N"-shaped input characteristic of a point-contact transistor designed for switching applications and the circuit used in obtaining it are shown in Fig. 1.[1,2] The emitter voltage, V'_e, is supplied from a constant-current source having a very high internal impedance. When such a supply is used, any change in the input impedances of the transistor is negligible in comparison with the impedance of the supply. The input characteristic curve shown in Fig. 1(b) covers an operating range in which the emitter current, I_e, is varied from a negative value through zero to a large positive value. In the region between the points P_1 and P_2, the current amplification factor, α, from the emitter to the collector is high; as a result, there is high positive feedback in this region and the collector current, I_c, changes much faster than the emitter current, I_e. Although both currents are present in the base circuit, they flow in opposite directions. The base current, I_b, is equal to the difference between the collector current and the emitter current. The base current flows in the same direction as the collector current because the collector current is larger than the emitter current due to the action symbolized by the internal generator shown in Fig. 1(a). The resultant voltage across the total base resistance, $r_b + R_b$, is in phase with the voltage between emitter and base, V'_e. Therefore, as the emitter current, I_e, increases, the base current, I_b, increases in the opposite direction, producing positive feedback. In the region of the curve beyond point P_2, the collector circuit reaches saturation, the current amplification factor, α, approaches zero, the negative base current decreases, and the input impedance is again positive. In effect, the transistor becomes a passive network.

The "N"-shaped input characteristic curve may be divided into three separate regions, as shown in Fig. 1(b). These regions may be called the "cutoff" region, the "transition" region, and the "saturation"

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RADIO CORPORATION OF AMERICA, HARRISON, NEW JERSEY

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region. In the "cutoff" region, the slope of the curve, which is equivalent to the input impedance of the transistor, is equal to the sum of the internal emitter resistance, r_e, the internal base resistance, r_b, and the external base resistance, R_b. The internal emitter resistance, r_e, in this region, however, is effectively the back impedance of a diode and is so large that the effect of the total base resistance, $r_b + R_b$, can be neglected. For all practical purposes, therefore, the slope or input impedance is equal to r_e. The point P_1 occurs when the emitter current, I_e, is effectively equal to zero. The location of this point is determined by the collector current which flows through the external base resistance, R_b. This resistance is assumed to be much larger than

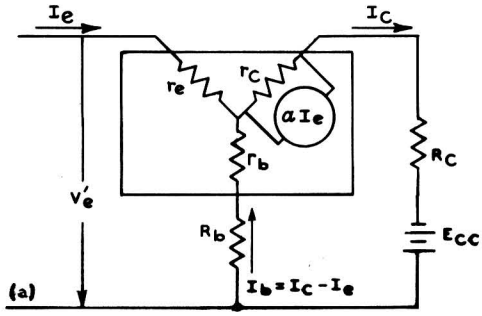

Fig. 1a - Test circuit used to obtain input characteristic of point-contact transistors.

$$\text{SLOPE I} = r_e + r_b + R_b \approx r_e$$

$$\text{SLOPE II} = r_e + (r_b + R_b)\left[\frac{(1-\alpha)\,r_e + R_c}{r_b + R_b + r_c + R_c}\right] \approx \frac{R_b\left[R_c + r_c\,(1-\alpha)\right]}{R_b + R_c + r_c}$$

$$\text{SLOPE III} = r_e + \frac{(R_b + r_b)(R_c + r_c)}{(R_b + r_b + R_c + r_c)} \approx \frac{R_b R_c}{R_b + R_c}$$

$$\text{At } P_2,\ V'_e = \frac{R_b\,(1-\alpha)\,E_{cc}}{\alpha\,(R_b + R_c) - R_b}$$

$$\text{At } P_2,\ I_e = \frac{E_{cc}}{\alpha\,(R_b + R_c) - R_b}$$

$$\text{At } P_3,\ I_e = \frac{R_b\,E_{cc}}{(r_e + R_b) + R_c} \approx \frac{E_{cc}}{r_c}$$

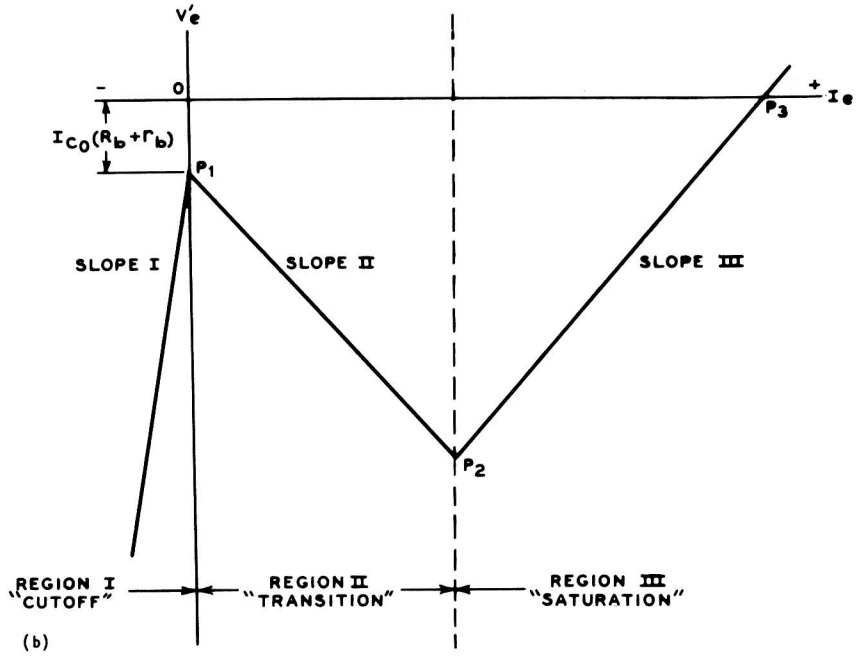

Fig. 1b - "N"-shaped input characteristic of point-contact transistors.

the internal base resistance, r_b. The point P_1 usually falls slightly to the right of the V'_e axis because the current amplification factor does not become greater than unity until the emitter current is very slightly positive.

In the "transition" region, where the emitter current is positive, the internal emitter resistance, r_e, is effectively that of a diode biased in its forward direction and has a very small value. This resistance, therefore, may be neglected in the calculations for both the "transition" and the "saturation" regions. The slope of the curve in the transition region is approximately equal to:

$$\frac{R_b\left[R_c + r_c\ (1 - \alpha)\right]}{R_b + R_c + r_c}$$

The point P_2 is mathematically located at the point where the emitter current, I_e, is equal to:

$$\frac{E_{cc}}{\alpha\ (R_b + R_c) - R_b}$$

and the emitter voltage, V'_e, is equal to:

$$\frac{R_b\ (1 - \alpha)\ E_{cc}}{\alpha\ (R_b + R_c) - R_b}$$

The current amplification factor, α, used in these calculations is measured at a point very close to the knee of the collector characteristic.

In the "saturation" region, the internal collector resistance, r_c, is small in comparison to the external parameters, $R_c + R_b$, and may be neglected in the calculations for this region of the input characteristic. The current amplification factor, α, in this region is theoretically zero. For all practical purposes therefore, the slope and the point P_3 are determined by external circuit parameters alone. The slope of the curve in this region is approximately equal to:

$$\frac{R_b R_c}{R_b + R_c}$$

The point P_3 is located approximately at the point where the emitter voltage, V'_e, is equal to zero and the emitter current, I_e, is approximately at the point where the emitter voltage, V'_e, is equal to zero and the emitter current, I_e, is approximately equal to E_{cc}/R_c.

Output Characteristic

The output characteristic shown in Fig.2(a) is somewhat idealized, particularly in the "knee" or low-collector-voltage region. In the low-resistance portion of the curve below the "knee", it is assumed that the collector-current function is constant for various values of emitter current and that a current amplification factor of zero is produced in this region. Because the "knee" of the collector characteristic changes abruptly, the current amplification factor also changes abruptly from zero to its rated value and the collector resistance from low to high values. Actual transistors have a rounded "knee", as shown in the 2N32 collector characteristic in Fig.2(b), but this degree of departure does not appreciably affect the practical value of this analysis. If the transistor's "knee" characteristic should become even less pronounced, the value of the analysis naturally is adversely affected, as is the

performance of the unit in switching service. Usually, the "knee" of the 2N32 occurs at a collector voltage of approximately 5 volts.

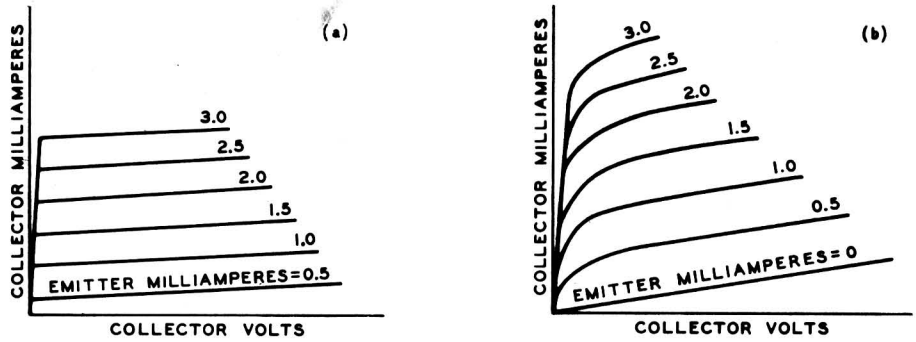

Fig. 2 - Idealized output characteristic for point-contact transistor (a), and output characteristic of 2N32 (b).

Monostable Operation

By definition, a monostable circuit is stable in only one state, either ON or OFF. The circuit to be discussed here is stable in the OFF state. For this type of operation, it is necessary that a dc load line intersect the input characteristic only at one point in the "cut-off" region. In the circuit shown in Fig. 3(a), the capacitance C determines this dc load line. The function of the resistance R_1 in this circuit is to apply a negative dc bias current to the emitter, shifting the "N"-shaped input curve so that the point P_1 falls in the region of positive emitter current.

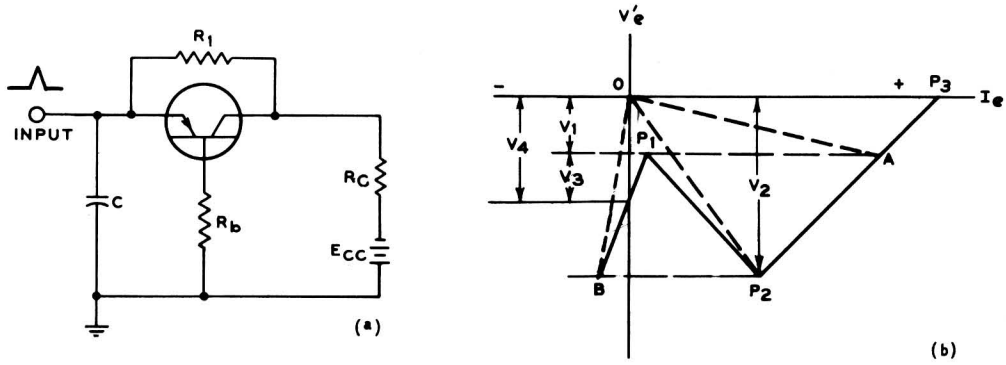

Fig. 3 - Circuit (a) for monostable operation of transistor, and curve (b) showing load line for typical unit.

Under dc conditions, the capacitor C charges to a fixed value, V_4, as shown in Fig. 3(b), and the emitter draws a reverse current through resistor R_1. The "cutoff" region represents the only stable portion of the input characteristic. If a positive voltage pulse having a value greater than V_3 is then applied to the emitter, the circuit is triggered into the "transition" region, where a great amount of positive feedback

is present. At the instant of change from one region to the other, the capacitor C is practically a closed circuit and determines the load line OA. This load line intercepts the input curve in the "saturation" region at a value of emitter voltage equal to V_1, or the charge on the capacitor. During transition, the capacitor C may also be considered to be short-circuited to a battery having a potential equal to V_1. When the emitter starts drawing current, the capacitor C charges to a value equal to V_2. The load line OA then shifts in a clockwise direction to the position OP_2. At this point, the high feedback of the "transition" region causes the load line to jump to a position having a value equal to V_2 and intercepting the input characteristic in the stable "cutoff" region at the point B. The capacitor C then discharges through the external base resistance, R_b, in series with the back impedance of the emitter which is the internal emitter resistance, r_e, in the "cutoff" region. The load line OB then shifts in a counter-clockwise direction until it coincides with the V'_e axis, and the cycle is completed.

The time constant,

$$\frac{R_b R_c}{R_b + R_c} C,$$

and the actual location of the point P_2 determine the ON time of the circuit. P_2 may vary considerably from unit to unit or may change during life, thus changing the time duration of the output pulse considerably. The monostable circuit, however, is used primarily as a

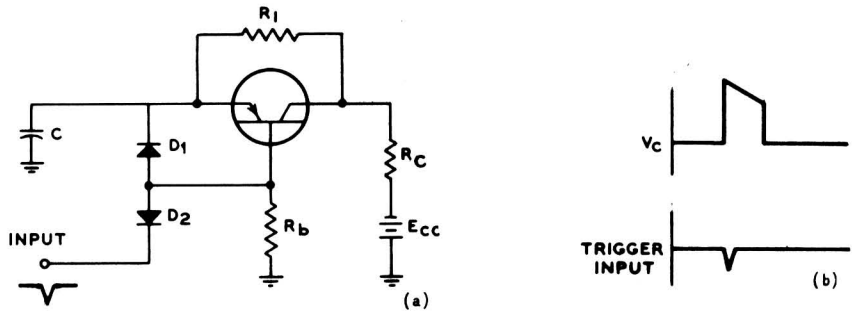

Fig. 4 - Circuit (a) incorporating diode to improve triggering rate, and waveforms (b) of collector voltage and trigger pulse.

trigger source for other circuits in which the pulse-duration requirements are not stringent. The rate at which the circuit can be triggered is limited because of the relatively long time required for the capacitor C to discharge through the large back impedance of the emitter from a value equal to V_2 to a value equal to V_4. This triggering rate can be greatly improved by the use of diode, D_1, as shown in Fig. 4(a). When the emitter is negative with respect to the base, the diode D_2 is biased in the direction of its low impedances and shunts the input of the transistor. The capacitor C, therefore, effectively discharges through the external base resistance, R_b, alone, thus greatly reducing the discharge time.

The circuit shown in Fig.4(a) is triggered by a negative pulse in the base which produces the same effect as a positive pulse applied to the emitter. Fig.4(b) shows the waveforms of the collector voltage and the trigger pulse. Diode D_2 is connected so that it conducts only when the input pulse is present. This arrangement has the advantage of providing a low input impedance only during trigger applications and a very high input impedance throughout the remainder of the cycle.

The triggering rate is also limited by hole-storage effects of the collector in the "saturation" region, as well as by the magnitude of the collector current, I_e, and the length of time the transistor operates in this region. A point-contact transistor normally requires about 0.25 microsecond for recovery. Because of the variation of hole mobility with collector voltage, the recovery time varies appreciably from unit to unit. The collector-current rise time is closely related to the variation of current amplification factor with frequency and is quite rapid for transistors like the 2N32. A value of 0.05 microsecond is normal for the rise of collector current.

Bistable Operation

The fundamental requirement for bistable operation is that a resistive load intersect the input characteristic at three points, one in each region. In a bistable circuit, a transistor is stable in both its ON and OFF states and can be switched from one stable state to the other upon the application of a trigger pulse. Fig.5(a) shows a bistable circuit having an emitter load resistance R_e. The function of the battery E_{ee} in this circuit is to shift the load line in the negative direction so that it intersects the input characteristic as shown in Fig.5(b). When a trigger pulse having a value greater than V_1 is applied to the emitter, the circuit is triggered into the "transition"

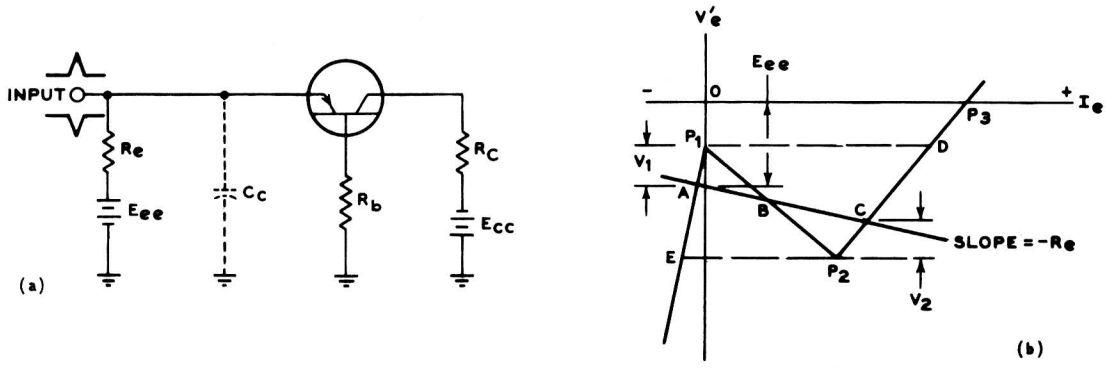

Fig.5 - Circuit (a) for bistable operation of transistor, and curve (b) showing load line for typical unit.

region. The internal and circuit capacitances react in the same way as capacitor C in Fig.3(a), and the current changes almost instantly from the value at P_1 to that at D. As the distributed capacitance charges, the operating point shifts on the input characteristic until it reaches point C. Because the distributed capacitance is extremely small, the path of operation from P_1 to D to C is practically instantaneous. The

circuit is stable at point C until a negative pulse having a value greater than V_2 is applied to the emitter. It is then triggered through the unstable region and becomes stable again at point A.

At the present time, the variation between individual transistors and the shift of certain characteristics during life present a problem to the circuit designer. For example, a change in the collector current at zero emitter current, Ic_o, causes a shift in the input characteristic of a transistor even though the other internal parameters remain constant. The value of Ic_o not only varies between units and with life, but also increases with increasing ambient temperature and changes radically at temperatures above 60 degrees Centigrade. This variation can easily render the circuit inoperative unless special biasing methods are employed.

Fig.6(a) shows the input characteristics for two transistors of the same type. As shown in this figure, the difference between the input characteristics of transistor 1 and transistor 2 causes the point P_1 to move on the V'_e axis, so that the load AB fails to intersect the curve for transistor 2 in the three places required for proper operation. Although the load line A'B' intersects both curves in the three desired regions, nearly twice as much trigger pulse would be required to trigger transistor 1 as to trigger transistor 2. Because the location of the point P_2 and the slope of the input characteristic in the "transition" region also vary considerably between units, and for individual units during life, a circuit must be designed to accommodate a range of characteristics such as that shown by the shaded area in Fig.6(b). It is apparent that a simple bistable circuit could not use all transistors occupying this range.

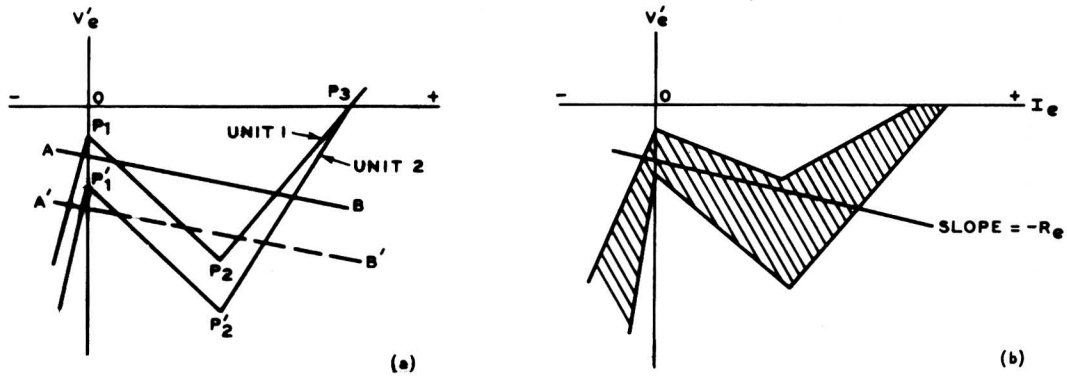

Fig. 6 - Curves showing input characteristics for two typical transistors of same type (a), and range of input characteristics for transistors of one type (b).

Certain circuit arrangements, however, can be used to obtain proper operation of a bistable circuit over a wide range of transistor characteristics. Fig.7(a) shows a circuit in which a crystal diode is used as the emitter load. Battery E_{bb} supplies a bias voltage between emitter and base which shifts the entire range of characteristics in the positive direction and centers it around the I_e axis. The diode, which provides

the composite load line AOB in Fig.7(b), has a very high impedance when the emitter current, I_e, is negative and a very low impedance when I_e is positive. This circuit accommodates a much larger range of units than one in which a pure resistive load is used.

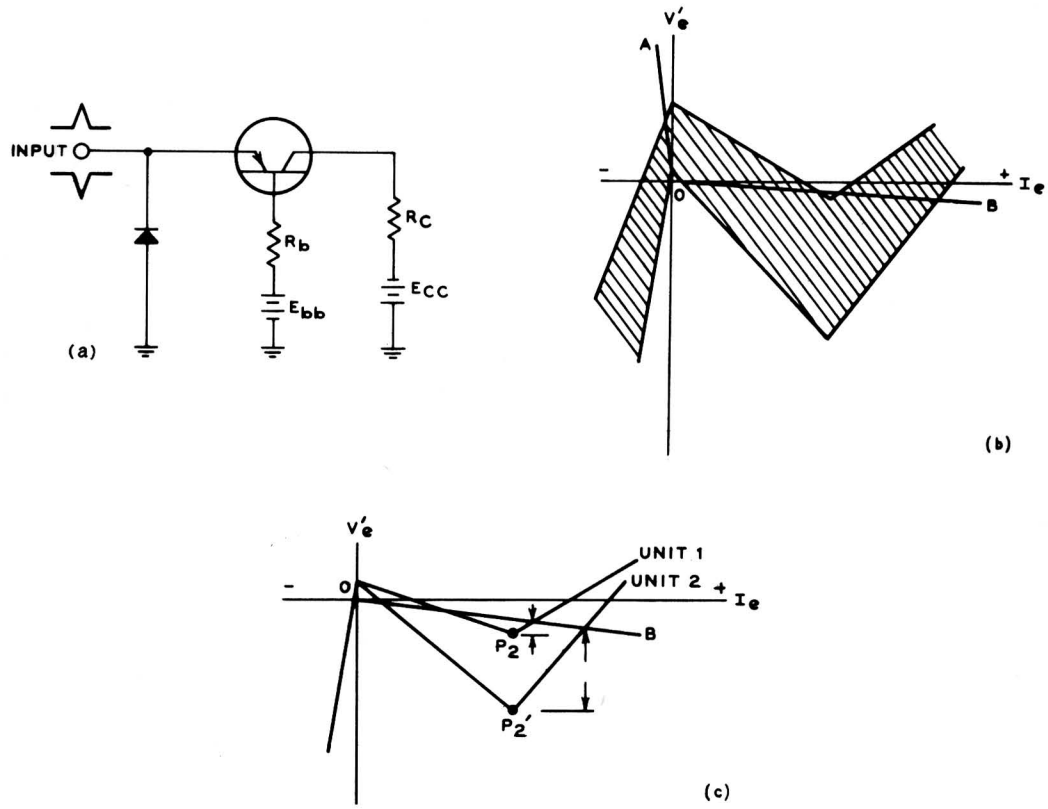

Fig. 7 - Bistable circuit (a) incorporating diode to accommodate full range of input characteristics, and curves showing load line in center of range (b) and for two typical units (c).

The magnitude of the pulse required to trigger a bistable circuit from ON to OFF is determined by the location of point P_2. Fig.7(c) shows two "N"-shaped input curves intersected by a portion of the diode load line discussed above. It can be seen that a much smaller pulse is required to trigger transistor 1 from ON to OFF than to trigger transistor 2. The location of the point P_2 is subjected to some variation between individual transistors and during life.

The input impedance of the transistor in the "cutoff" region should be quite high so that a voltage supplied by a high-impedance, low-power source can trigger the circuit. However, because a compromise between signal impedance and noise immunity may be desirable, the signal-source and input impedance may be reduced to prevent spurious noise voltages from triggering the circuit. Although noise pulses sometimes develop high peak voltage, they are relatively short in duration and cannot deliver an appreciable amount of power. In some applications it may be desirable for increased reliability to shunt the emitter circuit with a

resistor to decrease the input impedance, thereby increasing the amount of power required to trigger the circuit. This arrangement also makes the circuit less susceptible to the effects of variations in the back resistance of the emitter.

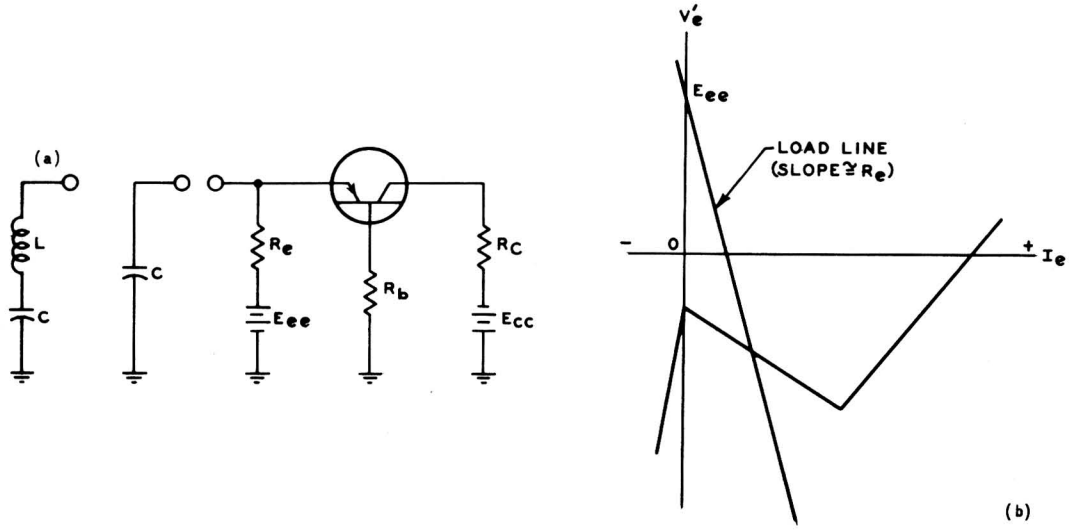

Fig. 8 - Astable circuit (a) and curve (b) showing dc load line established in emitter circuit.

Astable Operation

In astable operation, a circuit cannot be stable in any state. In such operation, the dc load line must intersect the input characteristic only at one point in the "transition" region. Three circuit arrangements which satisfy this requirement are shown in Figs. 8 through 10. Fig. 8(a) shows a circuit in which the reactive components are used to establish the dc load line for the emitter circuit. Fig. 9(a) shows a circuit in which the reactive components are used to form a load line in the

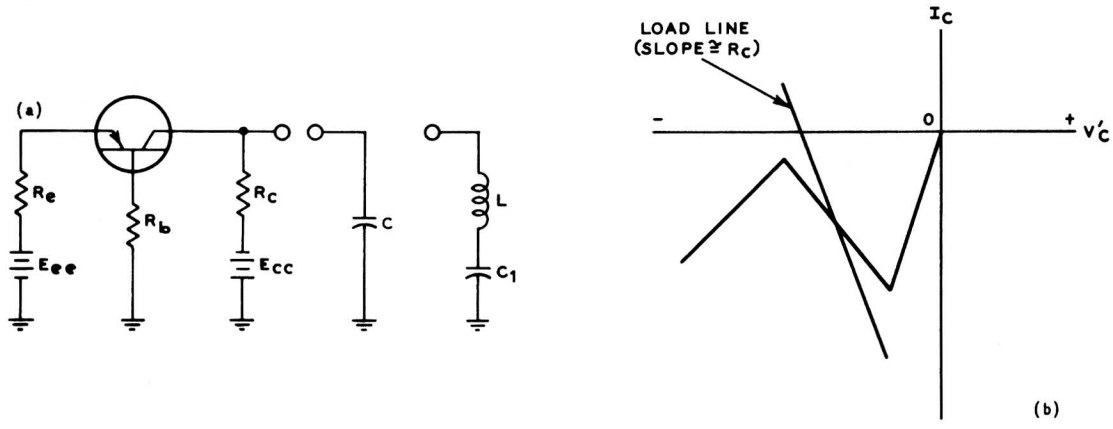

Fig. 9 - Astable circuit (a) and curve (b) showing dc load line established in collector circuit.

collector circuit. In this circuit, the capacitance C_1 may be used in series with the inductance L to form a resonant circuit which provides a sine-wave output voltage, or the capacitance may be used alone to provide a sawtooth voltage across its terminals or a pulse voltage across the base resistor. The circuit shown in Fig. 10(a) employs the reactive components to form a dc load line in the base circuit. A parallel-tuned circuit may be used to obtain sine-wave oscillation, or an inductance may be used to obtain sawtooth operation.

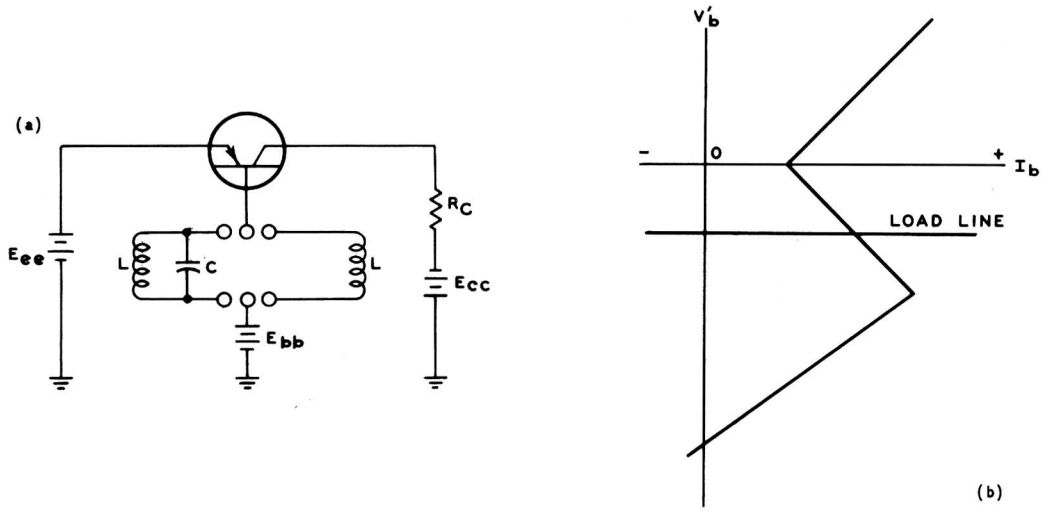

Fig. 10 - Astable circuit (a) and curve (b) showing dc load line established in base circuit.

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1 - A. W. Lo, *"Transistor Trigger Circuits"*, Proceedings of the I.R.E., Volume 40, Number 11, pp 1531 to 1541, November 1952.

2 - R. M. Ryder and R. J. Kirchner, *"Some Circuit Aspects of the Transistor"*, Bell System Technical Journal, Volume 28, pp 367 to 400, July 1949.